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| **D**epartment of **C**omputer **E**ngineering | Subject : Computer System  Class :…ICT K57……………………  Fullname :…………………………………… Student Index:……….. | Exam ID |
|  | *Duration:* ***60 minutes*** *Date: 22/11/2016*  *Allow student to use paper documents*  *Each question has a correct option. Not decrease mark for wrong answer Should write the choice into Answer Part, others are illegal.* | 2016B |

# ANSWER PART

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Question** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** |
| **Answer** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

# QUESTIONAIRE

**Question 1.** Consider a 256-byte cache with 8-byte blocks, an associativity of 4 and LRU block replacement. The cache is physically tagged. The processor has 32-KiB of physical memory. What is the number of tag bits?

(A) 8 bits (B) 9 bits (C) 10 bits (D) 11 bits

**Question 2.** Assume that there is a physical memory 64KiB, the virtual memory with the address length of 17 bit uses 128-bytes pages. What is the **wrong answer?**

(A) 512 Physical Pages (B) 1024 Virtual Pages (C) 128 Ki Physical Pages (D) Not enough infomation

**Virtual** Page Number

Page Offset

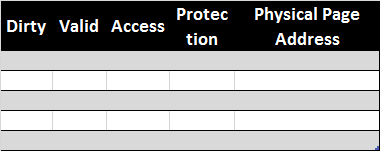
[ ?] .............................. [ ?] [ ?] ….... 2 1 0

**Physical** Page Number

Page Offset

Translation

[ ?] ................... [ ?] [ ?] ….... 2 1 0



Page Table

[ ?]

[ ?]

***HINT for Q2, 3***

**Question 3.** Assume that there is a physical memory 64KiB, the virtual memory with the address length of 17 bit uses 128-bytes pages. Calculate the size of page table given that each page requires more 4 protection bits (dirty bit, valid bit, accessed bit, protection level bit), and entries must be an integral number of bytes?

(A) 8 KiB (B) 4 KiB (C) 2 KiB (D) 1 KiB

**Question 4.** For a data cache with a 85% hit rate and a 1-cycle hit latency, calculate the average memory access latency. Assume that latency to memory and the cache miss penalty together is 140 cycles. Note: The

cache must be accessed after memory returns the data.

(A) 22.0 cycles (B) 18.5 cycles (C) 20.00 cycles (D) 11.92 cycles

**Question 5.** A computer is designed to enable 8-stages pipeline control so that each instruction can be completed in 8 cycles. How many cycles are needed to completely execute a software has 17 none-hazard instructions? Here, all instructions can be executed without being stopped halfway.

(A) 20 (B) 21 (C) 24 (D) 25

**Question 6.** Pipeline hazard issues occur at some lines in the source code below. Which of the following **warning is wrong**?

|  |  |  |
| --- | --- | --- |
|  | .set noreorder | (A) Data Hazard between line 2-3 |
| *1* | li t1, 2016 // assign |  |
| *2* | lw t2, 4(t1) // load from memory | (B) Control Hazard at line 4 |
| *3* | lw t3, 0(t2) // load from memory |  |
| *4* | beq t1, t3, skip // compare | (C) Data Hazard at line 3-4 |
| *5* | sw t2, 0(t1) // store into memory |  |
| *6* | skip: and t3, t1, t2 // simple operation | (D) Data Hazard at line 5-6 |

**Question 7.** Which of the following is superscalar architecture?

(A) (B)

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

(C) (D)

IF

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MEM

WB

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ID

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**Question 8.** Which hazard does Forwading method resolve?

(A) Data Hazard (B) Structure Hazard (C) Control Hazard (D) Data & Structure Hazard

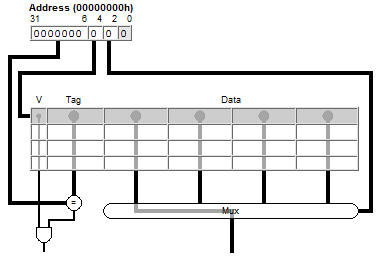
**Question 9.** Where is the Page Table module?

(A) Cache Memory (B) CPU (C) Main Memory (D) Hard disk

**Question 10.** Which kind of cache is the most appropriate with the below figure?

(A) 2-way cache (B) 4-way cache

(C) direct mapped cache (D) full associative cache



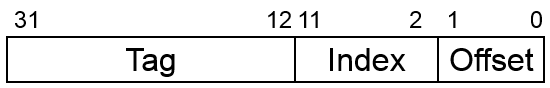
**Question 11.** A DRAM with 4-bank interleaved memory. The width of each bank is 1 byte. Bus width is 16 bit. The latency for address transfer is 3 cycles, for DRAM access is 22 cycles, and for data transfer from DRAM to cache is 3 cycles. How many cycles is taken for tranfer an 8-byte block?

(A) 48 (B) 55 (C) 58 (D) 59

**Question 12.** A DRAM with 4-bank interleaved memory. Bus width is 32 bit. Miss rate = 6%. Which bank does the address 0x824FCA belong to?

(A) 0 (B) 1 (C) 2 (D) 3

**Question 13**. The meaning of address bits as figure below. Here, cache is direct mapped. How large is the block size?



(A) 4 KiB (B) 2 KiB (C) 12 Byte (D) 4 Byte

**Question 14**. The table following is TLB. CPU must read from the virtual address 0x4A1B. How is status?

20 bits

12 bit

*Virtual Address*

|  |  |  |
| --- | --- | --- |
| Valid bit | Tag | Physical Page Number |
| 1 | 11 | 12 |
| 0 | 7 | 4 |
| 1 | 3 | 6 |
| 0 | 4 | 9 |

Hit, or miss, or unknown?

On disk, or on physical mem and what is the physical address?

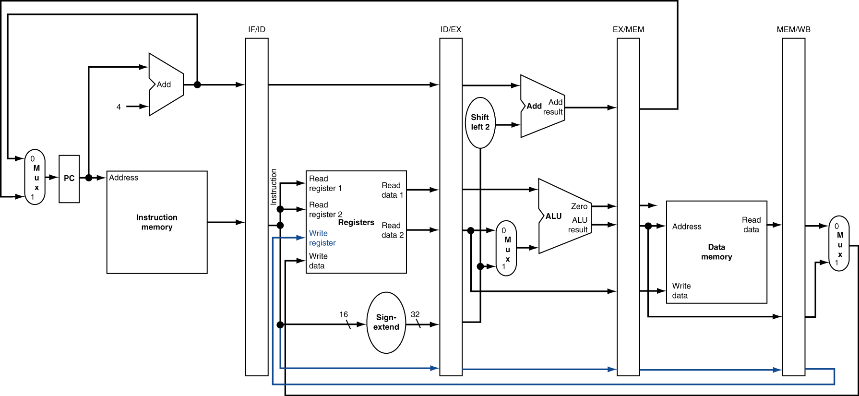
**Question 15.** In the pipeline figure below, the pipeline has 5 instructions with format op rd, rs1, rs2

At **ID stage**, which register is Read Register 1?

(A) $8 (B) $11 (C) $5 (D) $14

**Question 16**. In the pipeline figure below, at **ID stage**, which register is Write Register?

(A) $3 (B) $15 (C) $10 (D) $13



add $3, $2, $1 xor $6, $5, $4 xor $9, $8, $7 sub $12, $11, $10 and $15, $14, $13

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**Question 14**. Pay attention to V bit. V=1 mean that: the block data already exist on physical memmory. V=0 mean that: the block data is on disk only, not on physical memory. Within a row in TLB, tag contains virtual page number, and physical page number is the page number of physical memory respectively.

The address 0x4A1B (we know that 12 lower-bits 0xA1B are page offset) belongs to page no. 0x4. With Tag = 0x4 = 11(10) 🡪 search in TLB, V bit =0, don’t care Physical page number 🡪 miss, on disk.